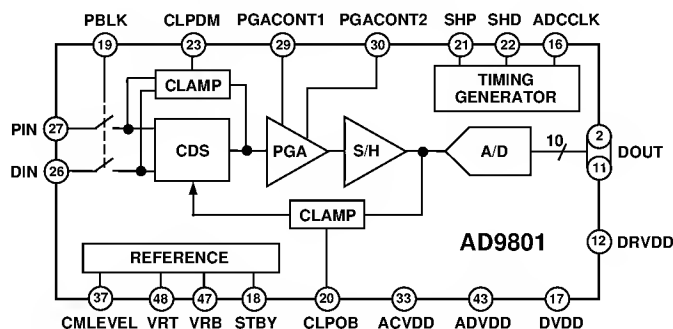


### FEATURES

**10-Bit, 18 MSPS A/D Converter**  
**18 MSPS Full-Speed CDS**  
**Low Noise, Wideband PGA**  
**Internal Voltage Reference**  
**No Missing Codes Guaranteed**  
**+3 V Single Supply Operation**  
**Low Power CMOS: 185 mW**  
**48-Pin TQFP Package**

### FUNCTIONAL BLOCK DIAGRAM



### PRODUCT DESCRIPTION

The AD9801 is a complete CCD signal processor developed for electronic cameras. It is well suited for both video conferencing and consumer level still camera applications.

The signal processing chain is comprised of a high speed CDS, variable gain PGA and 10-bit ADC. Required clamping circuitry and an onboard voltage reference are also provided. The AD9801 operates from a single +3 V supply with a typical power consumption of 185 mW.

The AD9801 is packaged in a space saving 48-pin thin-quad flatpack (TQFP) and is specified over an operating temperature range of 0°C to +70°C.

### PRODUCT HIGHLIGHTS

- On-Chip Input Clamp and CDS**  
 Clamp circuitry and high speed correlated double sampler allow for simple ac coupling to interface a CCD sensor at full 18 MSPS conversion rate.
- On-Chip PGA**  
 The AD9801 includes a low noise, wideband amplifier with analog variable gain from 0 dB to 31.5 dB (linear in dB).
- 10-Bit, High Speed A/D Converter**  
 A linear 10-bit ADC is capable of digitizing CCD signals at the full 18 MSPS conversion rate. (Typical DNL is  $\pm 0.5$  LSB and no missing code performance is guaranteed.)
- Low Power**  
 At 185 mW, the AD9801 consumes a fraction of the power of presently available multichip solutions. The part's power-down mode (15 mW) further enhances its desirability in low power, battery operated applications.
- Digital I/O Functionality**  
 The AD9801 offers three-state digital output control.
- Small Package**  
 Packaged in a 48-pin, surface-mount thin-quad flatpack, the AD9801 is well suited to very tight, low headroom designs.

REV. 0

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# AD9801—SPECIFICATIONS (T<sub>MIN</sub> to T<sub>MAX</sub> with ACVDD = 3.15 V, ADVDD = 3.15 V, DVDD = 3.15 V, DRVDD = 3.15 V unless otherwise noted)

Parameter	Min	Typ	Max	Units
TEMPERATURE RANGE				
Operating	0		70	°C
Storage	−65		150	°C
POWER SUPPLY VOLTAGE (For Functional Operation)				
ACVDD	3.00	3.15	3.50	V
ADVDD	3.00	3.15	3.50	V
DVDD	3.00	3.15	3.50	V
DRVDD	3.00	3.15	3.50	V
POWER SUPPLY CURRENT				
ACVDD		39.5		mA
ADVDD		14.6		mA
DVDD		4.7		mA
DRVDD		0.07		mA
POWER CONSUMPTION				
Normal Operation		185		mW
Power-Down Mode		15		mW
MAXIMUM SHP, SHD, ADCCLK RATE	18			MHz
ADC				
Resolution	10			Bits
Differential Nonlinearity		±0.5		LSB
No Missing Codes		GUARANTEED		
ADCCLK Rate			18	MHz
Reference Top Voltage		1.75		V
Reference Bottom Voltage		1.25		V
Input Range		1.0		V p-p
CDS				
Maximum Input Signal	500			mV p-p
Pixel Rate			18	MHz
PGA <sup>1</sup>				
Maximum Gain		31.5		dB
High Gain	15	19	23	dB
Medium Gain	0.5	3.5	6.5	dB
Minimum Gain	−5	−1	+3	dB
CLAMP				
Average Black Level (During CLPOB. Only Stable Over PGA Range 0.3 V to 2.7 V)		32		LSB

<sup>1</sup>PGA test conditions: max gain PGACONT1 = 2.7 V, PGACONT2 = 1.5 V; high gain PGACONT1 = 2.0 V, PGACONT2 = 1.5 V; medium gain PGACONT1 = 0.5 V, PGACONT2 = 1.5 V; minimum gain PGACONT1 = 0.3 V, PGACONT2 = 1.5 V.

Specifications subject to change without notice.

## DIGITAL SPECIFICATIONS (T<sub>MIN</sub> to T<sub>MAX</sub> with ACVDD = 3.15 V, ADVDD = 3.15 V, DVDD = 3.15 V, DRVDD = 3.15 V unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Units
LOGIC INPUTS					
High Level Input Voltage	V <sub>IH</sub>	2.4			V
Low Level Input Voltage	V <sub>IL</sub>			0.6	V
High Level Input Current	I <sub>IH</sub>		10		μA
Low Level Input Current	I <sub>IL</sub>		10		μA
Input Capacitance	C <sub>IN</sub>		10		pF
LOGIC OUTPUTS					
High Level Output Voltage	V <sub>OH</sub>	2.4			V
Low Level Output Voltage	V <sub>OL</sub>			0.6	V
	I <sub>OH</sub>		50		μA
	I <sub>OL</sub>		50		μA

Specifications subject to change without notice.

# TIMING SPECIFICATIONS (T<sub>MIN</sub> to T<sub>MAX</sub> with ACVDD = 3.15 V, ADVDD = 3.15 V, DVDD = 3.15 V, DRVDD = 3.15 V unless otherwise noted)

Parameter	Min	Typ	Max	Units
ADCCLK CLOCK PERIOD	55.6			ns
ADCCLK High Level Period	24.8	27.8		ns
ADCCLK Low Level Period	24.8	27.8		ns
SHP, SHD Clock Period	55.6			ns
Digital Output Delay		20		ns

## Digital Output Data Control

Mode1	Mode2	Digital Output Data (D9–D0)
0	0	Normal Operation
0	1	1   0   1   0   1   0   1   0   1   0
1	0	0   1   0   1   0   1   0   1   0   1
1	1	High Impedance

## ABSOLUTE MAXIMUM RATINGS\*

Parameter	With Respect To	Min	Max	Units
ADVDD	ADVSS, SUBST	–0.3	6.5	V
ACVDD	ACVSS, SUBST	–0.3	6.5	V
DVDD	DVSS, DSUBST	–0.3	6.5	V
DRVDD	DRVSS, DSUBST	–0.3	6.5	V
SHP, SHD	DSUBST	–0.3	DVDD + 2.0	V
ADCCLK, CLOB, CLPDM	DSUBST	–0.3	DVDD + 0.3	V
PGACONT1, PGACONT2	SUBST	–0.3	ACVDD + 0.3	V
PIN, DIN	SUBST	–0.3	ACVDD + 0.3	V
DOUT	DSUBST	–0.3	DRVDD + 0.3	V
VRT, VRB	SUBST	–0.3	ADVDD + 0.3	V
CLAMP_BIAS	SUBST	–0.3	ACVDD + 0.3	V
CCDBYP1, CCDBYP2	SUBST	–0.3	ACVDD + 0.3	V
STBY	DSUBST	–0.3	DVDD + 0.3	V
MODE1, MODE2	SUBST	–0.3	ADVDD + 0.3	V
DRVSS, DVSS, ACVSS, ADVSS	SUBST, DSUBST	–0.3	+0.3	V
Junction Temperature			+150	°C
Storage Temperature		–65	+150	°C
Lead Temperature (10 sec)			+300	°C

\* Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

## ORDERING GUIDE

Model	Temperature	Package Description	Package Option*
AD9801	0°C to +70°C	48-Pin TQFP	ST-48

\*ST = Thin Quad Flatpack Package.

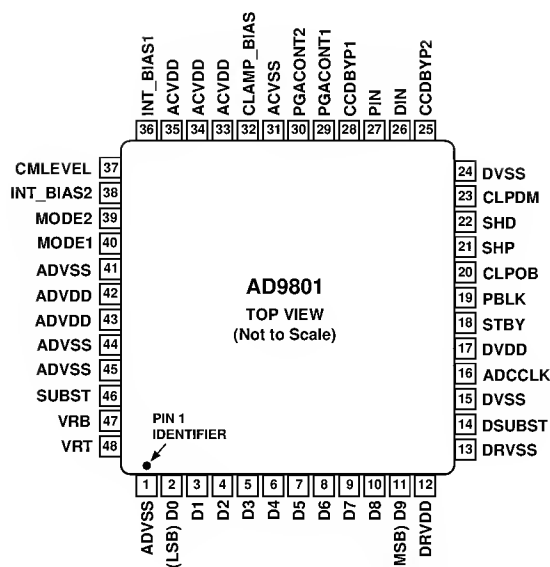
## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9801 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



# AD9801

## PIN CONFIGURATION



Pin No.	Pin Name	Type	Description
1	ADVSS	P	Analog Ground
2–11	D0–D9	DO	Digital Data Outputs
12	DRVDD	P	+3 V Digital Driver Supply
13	DRVSS	P	Digital Driver Ground
14	DSUBST	P	Digital Substrate
15	DVSS	P	Digital Ground
16	ADCCLK	DI	ADC Sample Clock Input
17	DVDD	P	+3 V Digital Supply
18	STBY	DI	Power down (Active HIGH)
19	PBLK	DI	Pixel Blanking (Active LOW)
20	CLPOB	DI	Black Level Restore Clamp (Active LOW)
21	SHP	DI	Reference Sample Clock Input
22	SHD	DI	Data Sample Clock Input
23	CLPDM	DI	Input Clamp (Active Low)
24	DVSS	DI	Digital Ground
25	CCDBYP2	AO	CCD Bypass (Decouple to Analog Ground Through 0.1 $\mu$ F)
26	DIN	AI	CDS Input (Tie to Pin 27 and AC-Couple to CCD Output Through 0.1 $\mu$ F)
27	PIN	AI	CDS Input (See Above)
28	CCDBYP1	AO	CCD Bypass (Decouple to Analog Ground Through 0.1 $\mu$ F)
29	PGACONT1	AI	Coarse PGA Gain Control (0.3 V–2.7 V Decoupled to Analog Ground Through 0.1 $\mu$ F)
30	PGACONT2	AI	Fine PGA Gain Control (0.3 V–2.7 V Decoupled to Analog Ground Through 0.1 $\mu$ F)
31	ACVSS	P	Analog Ground
32	CLAMP_BIAS	AO	Clamp Bias Level (Decouple to Analog Ground Through 0.1 $\mu$ F)
33	ACVDD	P	+3 V Analog Supply
34	ACVDD	AI	+3 V Analog Supply
35	ACVDD	AI	+3 V Analog Supply
36	INT_BIAS1	AO	Internal Bias Level (Decouple to Analog Ground Through 0.1 $\mu$ F)
37	CMLEVEL	AO	Common-Mode Level (Decouple to Analog Ground Through 0.1 $\mu$ F)
38	INT_BIAS2	AO	Internal Bias Level (Decouple to Analog Ground Through 0.1 $\mu$ F)
39	MODE2	DI	ADC Test Mode Control (See Digital Output Data Control)
40	MODE1	DI	ADC Test Mode Control (See Digital Output Data Control)
41	ADVSS	P	Analog Ground
42	ADVDD	P	+3 V Analog Supply
43	ADVDD	P	+3 V Analog Supply
44	ADVSS	P	Analog Ground
45	ADVSS	P	Analog Ground
46	SUBST	P	Substrate (Connect to Analog Ground)
47	VRB	AO	Bottom Reference Bypass (Decouple to Analog Ground Through 0.1 $\mu$ F)
48	VRT	AO	Top Reference Bypass (Decouple to Analog Ground Through 0.1 $\mu$ F)

## EQUIVALENT INPUT CIRCUITS

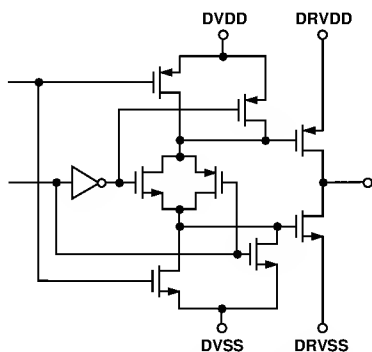


Figure 1. Pins 2-11 (DB0-DB9)

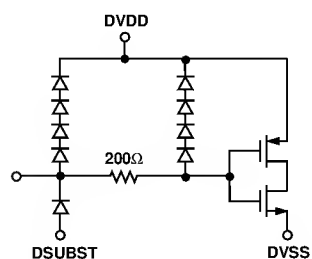


Figure 2. Pin 21 (SHP) and Pin 22 (SHD)

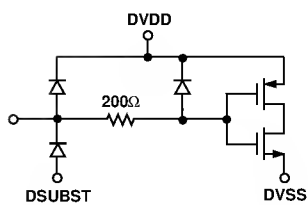


Figure 3. Pin 16 (ADCCLK)

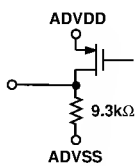


Figure 4. Pin 37 (CMLEVEL)

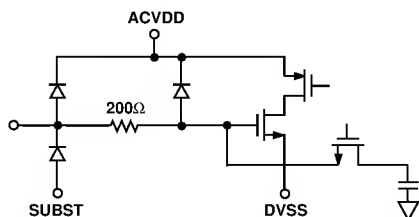


Figure 5. Pin 25 (CCDBYP2) and Pin 28 (CCDBYP1)

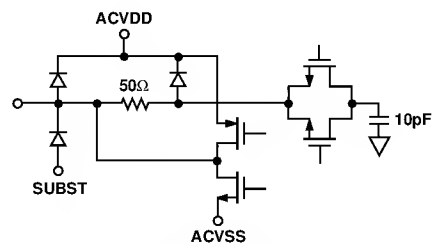


Figure 6. Pin 26 (DIN) and Pin 27 (PIN)

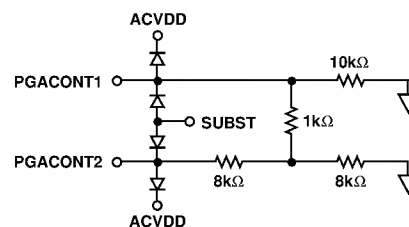


Figure 7. Pin 29 (PGACONT1) and Pin 30 (PGACONT2)

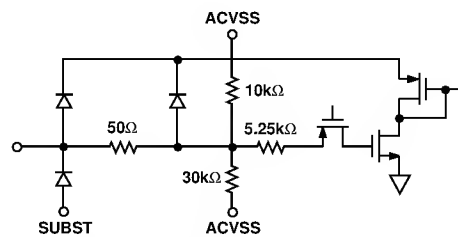


Figure 8. Pin 32 (CLAMP BIAS)

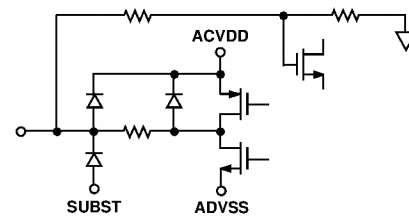


Figure 9. Pin 48 (VRT) and Pin 47 (VRB)

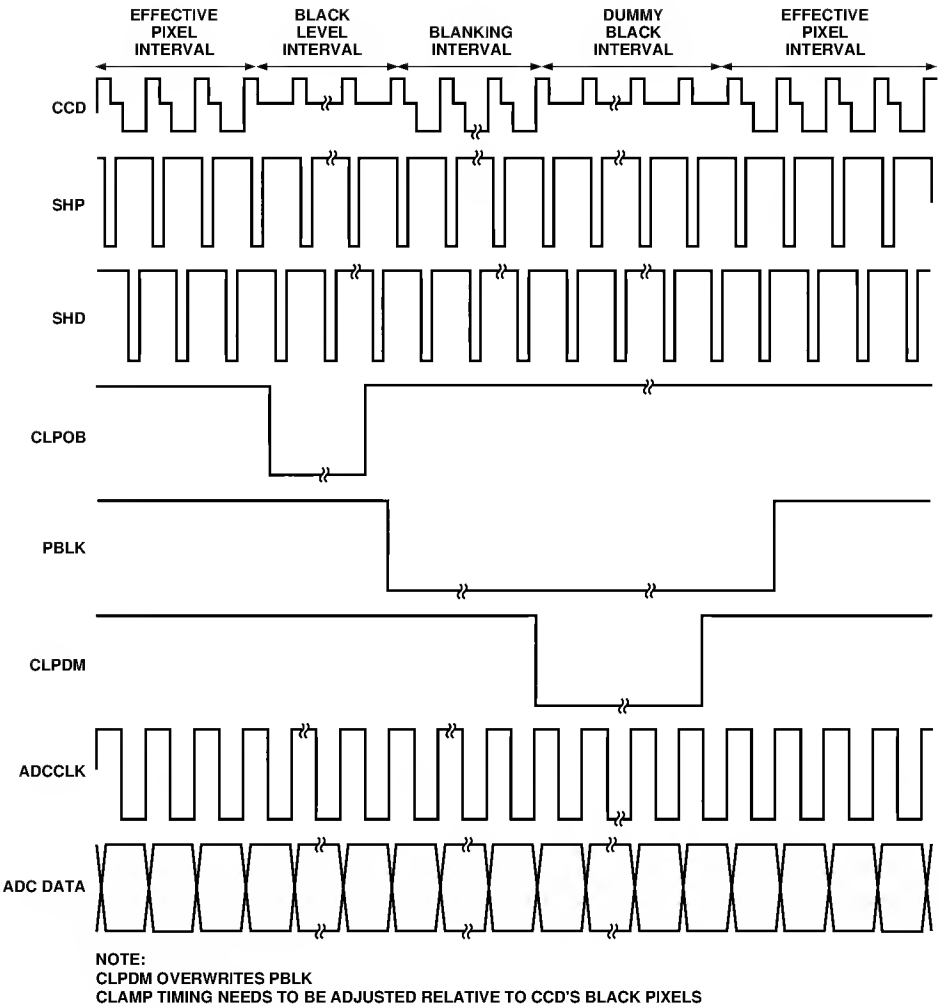


Figure 10. Typical Horizontal Interval Timing

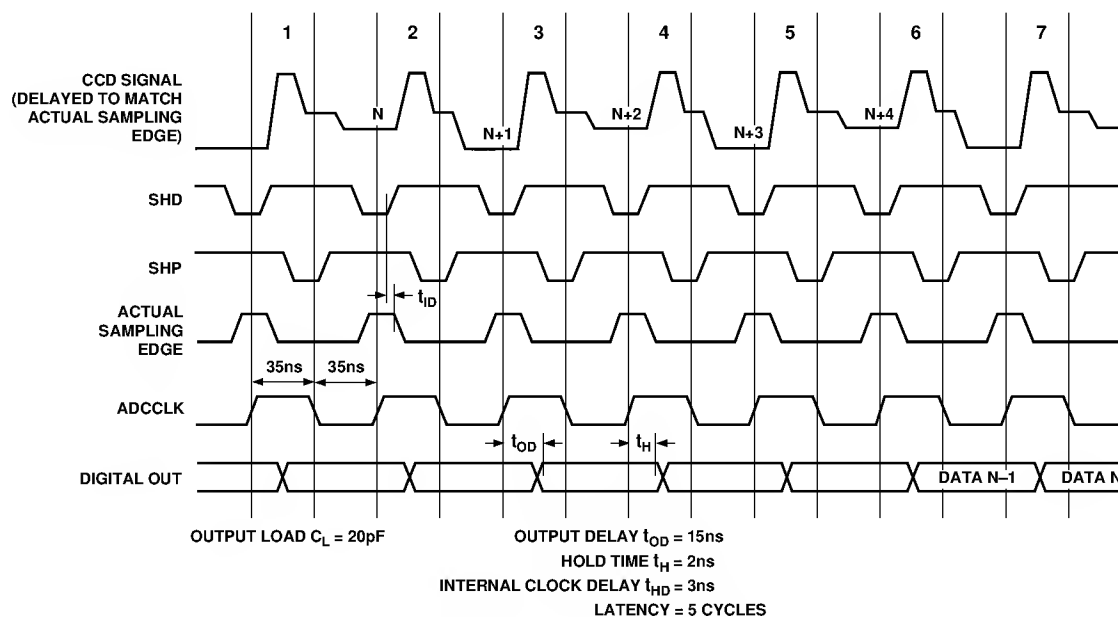


Figure 11. Timing Diagram

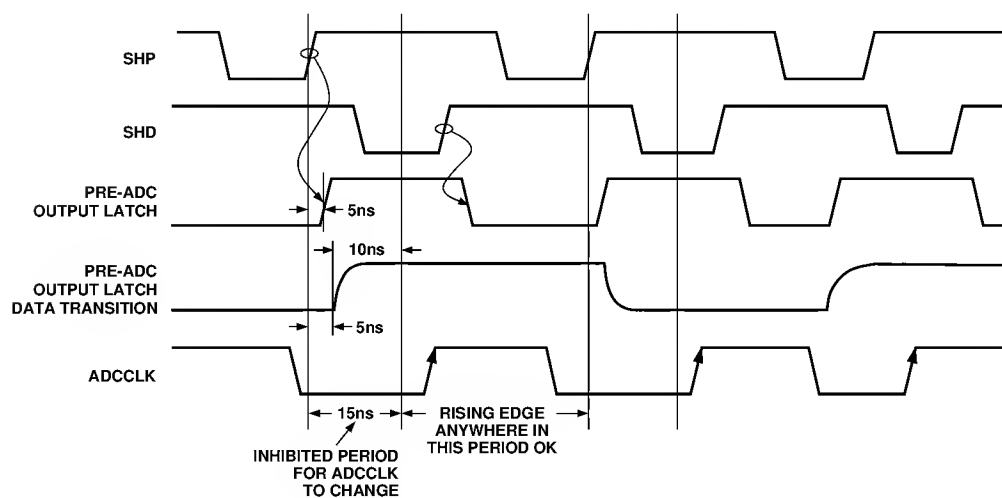


Figure 12. ADCCLK Timing Edge

# AD9801

## THEORY OF OPERATION

### Introduction

The AD9801 is a 10-bit analog-to-digital interface for CCD cameras. The block level diagram of the system is shown in Figure 13. The device includes a correlated double sampler (CDS), 0 dB–31 dB variable gain amplifier (PGA), black level correction loop, input clamp and voltage reference. The only external analog circuitry required at the system level is an emitter follower buffer between the CCD output and AD9801 inputs.

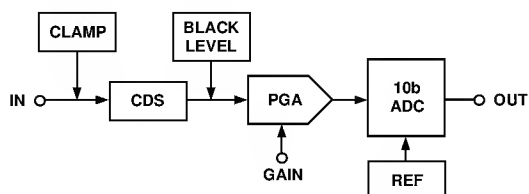


Figure 13.

### Correlated Double Sampling (CDS)

CDS is important in high performance CCD systems as a method for removing several types of noise. Basically, two samples of the CCD output are taken: one with the signal present (“data”) and one without (“reference”). Subtracting these two samples removes any noise that is common—or correlated—to both.

Figure 14 shows the block diagram of the AD9801’s CDS. The S/H blocks are directly driven by the input and the sampling function is performed passively, without the use of amplifiers.

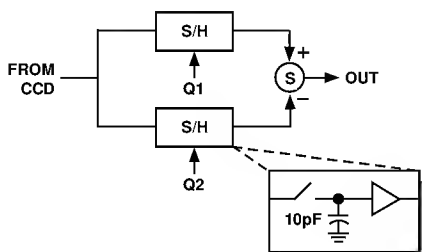


Figure 14.

This implementation relies on the off-chip emitter follower buffer to drive the two 10 pF sampling capacitors. Only one capacitor at a time is seen at the input pin.

The AD9801 actually uses two CDS circuits in a “ping pong” fashion to allow the system more acquisition time. In this way, the output from one of the two CDS blocks will be valid for an entire clock cycle. Thus, the bandwidth requirement of the subsequent gain stage is reduced as compared to that for a single CDS channel system. This lower bandwidth translates to lower power and noise.

### Programmable Gain Amplifier (PGA)

The on-chip PGA provides a (linear in dB) gain range of 0 dB–31.5 dB. A typical gain characteristic plot is shown in Figure 15. Only the range from 0.3 V to 2.7 V is intended for actual use.

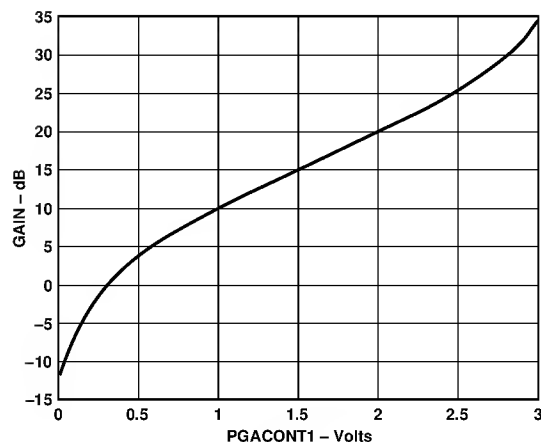


Figure 15.

As shown in Figure 16, PGA control is provided through the PGA CONT1 and PGA CONT2 inputs. PGA CONT1 provides coarse and PGA CONT2 fine (1/16) gain control.

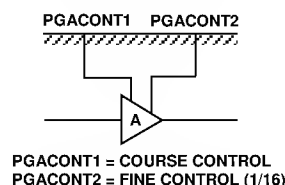


Figure 16.

### Black Level Clamping

For correct processing, the CCD signal must be referenced to a well established “black level” by the AD9801. At the edge of the CCD, there is a collection of pixels that are covered with metal to prevent any light penetration. As the CCD is read out, these “black pixels” provide a calibration signal that is used to establish the black level.

The feedback loop shown in Figure 17 is closed around the PGA during the calibration interval (CLPOB = LOW) to set the black level. As the black pixels are being processed, an integrator block measures the difference between the input level and the desired reference level. This difference, or error, signal is amplified and passed to the CDS block where it is added to the incoming pixel data. As a result of this process, the black pixels are digitized at one end of the ADC range, taking maximum advantage of the available linear range of the system.

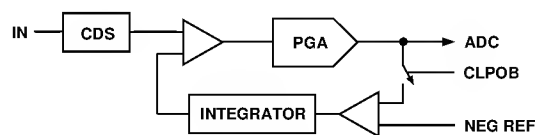


Figure 17.



The actual implementation of this loop is slightly more complicated as shown in Figure 18. Because there are two separate CDS blocks, two black level feedback loops are required and two offset voltages are developed. Figure 18 also shows an additional PGA block in the feedback loop labeled “RPGA.”

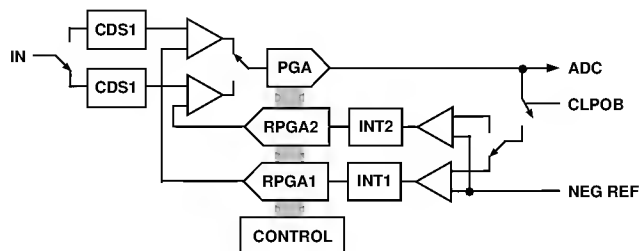


Figure 18.

The RPGA uses the same control inputs as the PGA, but has the inverse gain. The RPGA functions to attenuate by the same factor as the PGA amplifies, keeping the gain and bandwidth of the loop constant.

## Input Bias Level Clamping

The buffered CCD output is connected to the AD9801 through an external coupling capacitor. The dc bias point for this coupling capacitor is established during the clamping (CLPDM = LOW) period using the “dummy clamp” loop shown in Figure 19. When closed around the CDS, this loop establishes the desired DC bias point on the coupling capacitor.

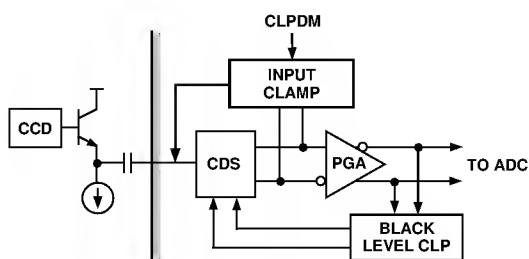


Figure 19.

## Input Blanking

In some applications, the AD9801’s input may be exposed to large signals from the CCD. These signals can be very large, relative to the AD9801’s input range, and could thus saturate on-chip circuit blocks. Recovery time from such saturation conditions could be substantial.

To avoid problems associated with processing these transients, the AD9801 includes an input blanking function. When active (PBLK = LOW), this function stops the CDS operation and allows the user to disconnect the CDS inputs from the CCD buffer.

If the input voltage exceeds the supply rail by more than 0.3 V, protection diodes will be turned on, increasing current flow into the AD9801 (see Equivalent Input Circuits). Such voltage levels should be externally clamped to prevent device damage or reliability degradation.

## 10-Bit Analog-to-Digital Converter (ADC)

The ADC employs a multibit pipelined architecture, which is well-suited for high throughput rates while being both area and power efficient. The multistep pipeline presents a low input capacitance resulting in lower on-chip drive requirements. A fully differential implementation was used to overcome headroom constraints of the single +3 V power supply.

## Differential Reference

The AD9801 includes a 0.5 V reference based on a differential, continuous-time bandgap cell. Use of an external bypass capacitor reduces the reference drive requirements, thus lowering the power dissipation. The differential architecture was chosen for its ability to reject supply and substrate noise. Recommended decoupling shown in Figure 20.

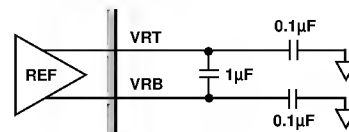


Figure 20.

## Internal Timing

The AD9801’s on-chip timing circuitry generates all clocks necessary for operation of the CDS and ADC blocks. The user needs only to synchronize the SHP and SHD clocks with the CCD waveform, as all other timing is handled internally. The ADCCLK signal is used to strobe the output data, and can be adjusted to accommodate desired timing.



## EVALUATION BOARD

Figure 22 shows the schematic for the AD9801 evaluation board. Notice the use of a common ground and supply for the AD9801, and the extensive supply and reference decoupling.

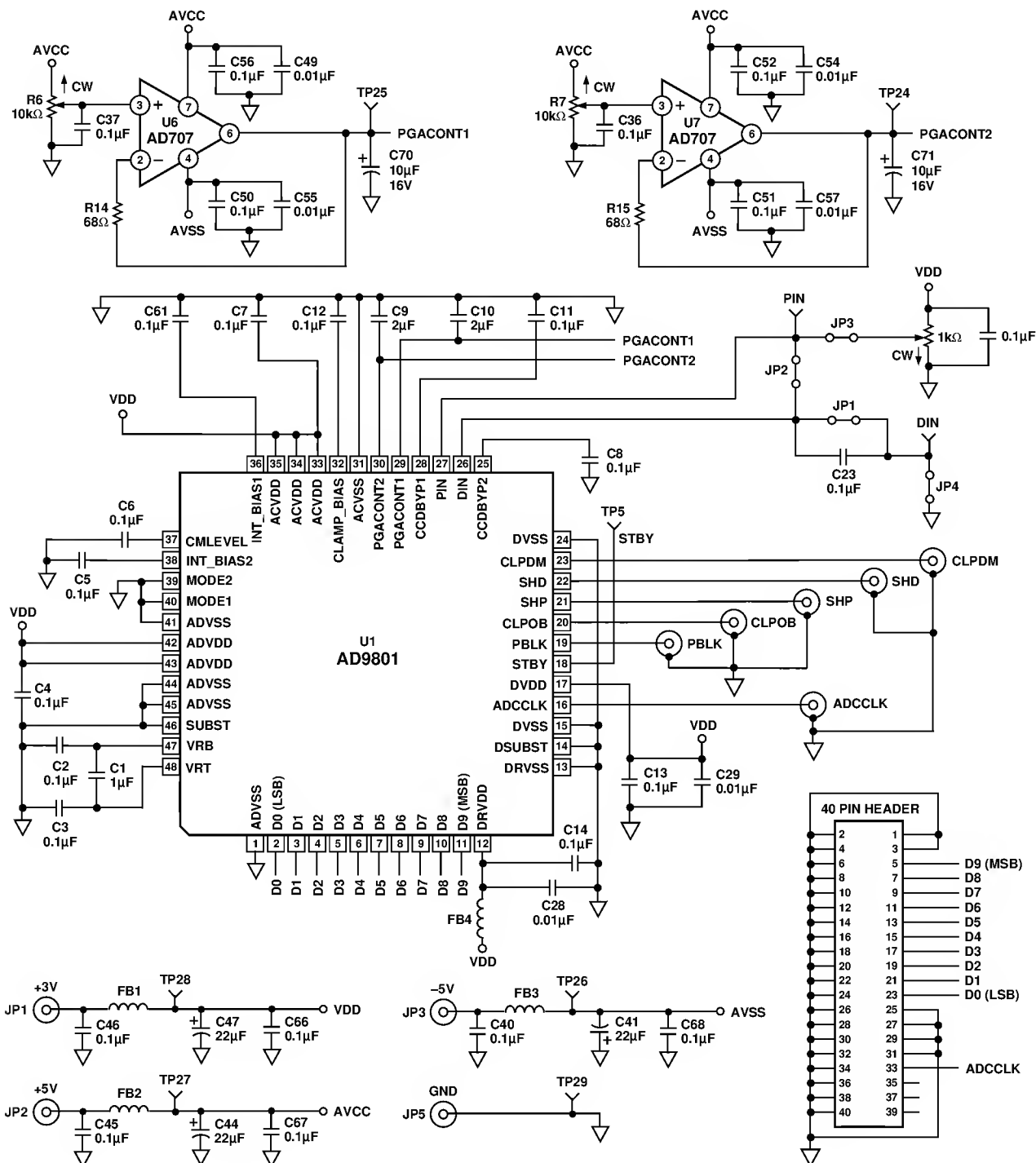
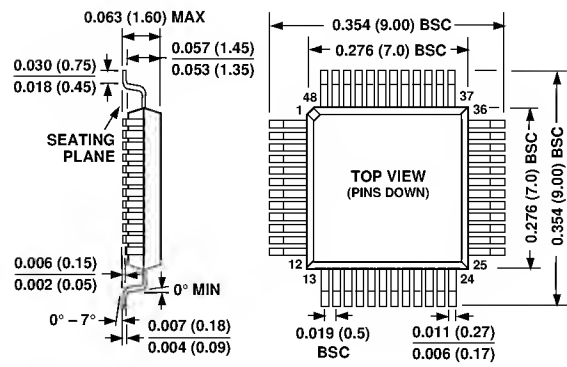


Figure 22. AD9801EB Schematic

OUTLINE DIMENSIONS  
Dimensions shown in inches and (mm).

48-Terminal Plastic Thin Quad Flatpack  
(ST-48)



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